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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/044,185	Applicant(s) KRAMER ET AL.
	Examiner JASON E. MATTIS	Art Unit 2461

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 11 December 2009.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)

Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

1. This Office Action is in response to the Request for Continued Examination filed 12/11/09. Claims 1-20 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 6-10, 13, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches (U.S. Publication US 2002/0110086 A1) in view of Fan (U.S. Pat. 5412648).

With respect to claims 1 and 8, Reches discloses a non-blocking crossbar and method of operation (**See page 2 paragraph 24 of Reches for reference to a crossbar switch and a method for controlling the crossbar switch such that packets are not blocked by each other**). Reches also discloses n inputs and n outputs (**See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports and N output ports**). Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of said n inputs and the

destination FIFO (See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed between a corresponding one of the N inputs and the destination FIFO). Reches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs (See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports). Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets (See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent). Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO

and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets.

With respect to claims 1 and 8, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet (**See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell**). Scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan, to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input

through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

With respect to claims 2 and 9, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof (**See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port**).

With respect to claims 3 and 10, Reches discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof (**See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels**).

With respect to claims 6 and 13, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO (**See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues**).

With respect to claims 7 and 14, Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority (**See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet**).

4. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Chen et al. (U.S. Pat. 6975638 B1).

With respect to claims 4, 5, 11, and 12, the combination of Reches and Fan does not specifically disclose that at least two of the n inputs are coupled to different types of packet based fabrics with the inputs and outputs being connected to a SONET network and two Ethernet networks.

With respect to claims 4, 5, 11, and 12, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network (See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network). A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches and Fan., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

5. Claims 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Hartmann et al. (U.S. Pat. 5905873).

With respect to claim 15, Reches discloses a multi-channel network line card for packet based networks (**See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a switch having input ports that correspond to a line multi-channel network line card**). Reches also discloses n physical interfaces and inputs numbering at least three (**See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports, which are physical interfaces, numbering at least three**). Reches further discloses a non-blocking crossbar coupled to the physical interfaces (**See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a configurable switch unit 50, which corresponds to a non-blocking crossbar coupled to the input ports**). Reches also discloses n outputs that transmit the packet to corresponding ones of the n physical interfaces (**See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N output ports transmitting packets to physical interfaces**). Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of the n inputs and the destination FIFO (**See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed**

between a corresponding one of the N inputs and the destination FIFOs. Reaches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs (**See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports**). Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets (**See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent**). Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets. Reches also does not specifically disclose n network processors that convert a packet between protocols coupled to corresponding ones of the n physical interfaces.

With respect to claim 15, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet (**See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell**). Scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan., to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

With respect to claim 16, Reches discloses a fast pattern processor that receives a packet from a physical interface and analyzes and classifies the packet (See page 3 paragraph 36 of Reches for reference to an input port receiving a packet and analyzing the packet to determine parameters including the priority of the packet, which is a classification of the packet). Reches does not disclose processing the packet and converting the packet into an appropriate network protocol.

With respect to claims 15 and 16, Hartmann et al., in the field of communications, discloses network processors coupled to corresponding physical interfaces that convert received packets between protocols (See the abstract of Hartmann et al. for reference to port adaptors, which are network processors, coupled to input ports, which are physical interfaces, that receive packets and convert them between different types of communication formats, which are protocols). Using network processors coupled to corresponding physical interfaces that convert received packets between protocols has the advantage of allowing all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets (See the abstract of Hartmann et al. for reference to this advantage).

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Hartmann et al., to combine using network processors coupled to corresponding physical interfaces that convert received packets between protocols, as suggested by Hartmann et al., with the system and method of

Reches and Fan, with the motivation being to allow all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets.

With respect to claim 17, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof (**See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port**). Reches also discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof (**See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels**).

With respect to claim 20, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO (**See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues**). Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority (**See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet**).

6. Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and Hartmann et al. and in further view of Chen et al.

With respect to claims 18 and 19, the combination of Reches, Fan, and Hartmann et al. does not specifically disclose that at least two of the n inputs are coupled to different types of packet based networks with the inputs and outputs being connected to a SONET network and two Ethernet networks.

With respect to claims 18 and 19, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network (**See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network**). A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches, Fan, and Hartmann et al., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

Response to Arguments

7. Applicant's arguments filed 12/11/09 have been fully considered but they are not persuasive.

Regarding Applicant's argument that Reches does not disclose that "each of the n crossbar FIFOs interposes a corresponding one of each of said n inputs and said destination FIFO", as currently claimed, the Examiner respectfully disagrees. The language of the claims in view of the teachings of Reches was discussed at length during an interview with the Applicant's representative on December 9, 2009. As stated by the Applicant's arguments it was agreed that "Reches only teaches that a FIFO interposes a destination FIFO and only one input". During the interview it was recommended that the claim language be changed such that it is clear that the claimed n crossbar FIFOs interpose a destination FIFO and every input. The current claim language does not include such a limitation. It is not clear how the claim language stating "each of the n crossbar FIFOs interposes a corresponding one of each of said n inputs and said destination FIFO" is different from the teachings of Reches that "a FIFO interposes a destination FIFO and only one input". According to the amended claim language, each of the n crossbar FIFOs interposes a corresponding one of each of the n inputs and the destination FIFO. Thus, the claim language only requires that each crossbar FIFO be between a single input (one of the multiple inputs) and the destination FIFO. As discussed in the interview on December 9, 2009 and as reiterated by the Applicant's arguments, Reches does disclose each FIFO interposing a single input and the destination FIFO. Therefore, the claim language has not been amended to overcome the rejections above.

In order to advance prosecution, a further search of the prior art was made in anticipation of the claims being amended such that they overcome the rejections above

based on Reches. It is believed that each of Ku et al. (U.S. Publication US 2002/0085545 A1), McKeown (U.S. Patent US 6,515,991 B1), and Cloonan et al. (U.S. Patent 5,724,352) disclose a crossbar switch with the same configuration of crossbar FIFO as described in the Applicant's specification and as illustrated by Figure 2 of the Applicant's drawings. Ku et al. discloses a non-blocking switch using a crossbar array that has buffers 618 that are equivalent to the claimed n crossbar FIFOs (See pages 5-6 paragraphs 61-62 and Figure 5 of Ku et al.). In the arrangement of Ku et al., the switch includes n input ports and n output port (with n being equal to 4 in the example of Figure 5) with each output port having n crossbar buffers 618 between the input ports and the output ports. Although Ku et al. does not specifically disclose a destination FIFO for each of the output ports, it is believed that the addition of a destination FIFO would be an obvious variation of the structure disclosed by Ku et al. McKeown discloses a crossbar switch including queues that are equivalent to the claimed n crossbar FIFOs (See column 3 line37 to column 4 line 32 and Figure 1 of McKeown). In the arrangement of McKeown, the switch includes n inputs and n outputs (with n being equal to 2 in the example of Figure 1) and a crossbar 120 whereby each output includes a queue, which is equivalent to the claimed destination FIFO, and whereby each output queue is connected to n corresponding crossbar queues of the crossbar 120 with each of the n crossbar queues being between the output queue and a different input. Cloonan et al. discloses a crossbar switch including pipes, which are equivalent to the claimed n crossbar FIFOs (See column 7 line 50 to column 8 line 8 and Figure 4 of Cloonan et al.). In the arrangement of Cloonan et al., the switch includes n input ports

and n output ports (with n being equal to 256 in the example of Figure 4) and a switch fabric 14 containing the pipes whereby each output port is connected to n corresponding pipes with each of the n pipes being between the output port and a different input port. Thus, it is believed that even if the claims were amended to overcome the teaching of Reches, the Applicant's invention as described in the specification and specifically the configuration as shown in Figure 2 of the Applicant's drawing would have been obvious in view of any one of Ku et al., McKeown, or Cloonan et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON E. MATTIS whose telephone number is (571)272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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